MC10E197

5V ECL Data Separator

The MC10E197 is an integrated data separator designed for use in high speed hard disk drive applications. With data rate capabilities of up to 50 Mb/s the device is ideally suited for today's and future state-of-the-art hard disk designs.

The E197 is typically driven by a pulse detector which reads the magnetic information from the storage disk and changes it into ECL pulses. The device is capable of operating on both 2:7 and 1:7 RLL coding schemes. Note that the E197 does not do any decoding but rather prepares the disk data for decoding by another device.

For applications with higher data rate needs, such as tape drive systems, the device accepts an external VCO. The frequency capability of the integrated VCO is the factor which limits the device to 50 Mb/s.

A special anti-equivocation circuit has been employed to ensure timely lock-up when the arriving data and VCO edges are coincident.

Unlike the majority of the devices in the ECLinPS family, the E197 is available in only 10H compatible ECL. The device is available in the standard 28-lead PLCC.

Since the E197 contains both analog and digital circuitry, separate supply and ground pins have been provided to minimize noise coupling inside the device. The device can operate on either standard negative ECL supplies or, as is more common, on positive voltage supplies.

- 2:7 and 1:7 RLL Format Compatible
- Fully Integrated VCO for 50 Mb/s Operation
- External VCO Input for Higher Operating Frequency
- Anti-equivocation Circuitry to Ensure PLL Lock
- PECL Mode Operating Range: V_{CC} = 4.2 V to 5.7 V with V_{EE} = 0 V
- NECL Mode Operating Range: V_{CC} = 0 V with V_{EE} = −4.2 V to −5.7 V
- Internal Input Pulldown Resistors
- ESD Protection: > 1 KV HBM, > 75 V MM
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL−94 code V−0 @ 1/8″,
  Oxygen Index 28 to 34
- Transistor Count = 483 devices

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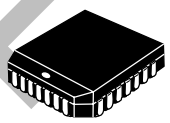
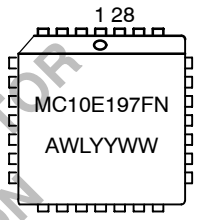


PLCC−28
CASE 776
FN SUFFIX

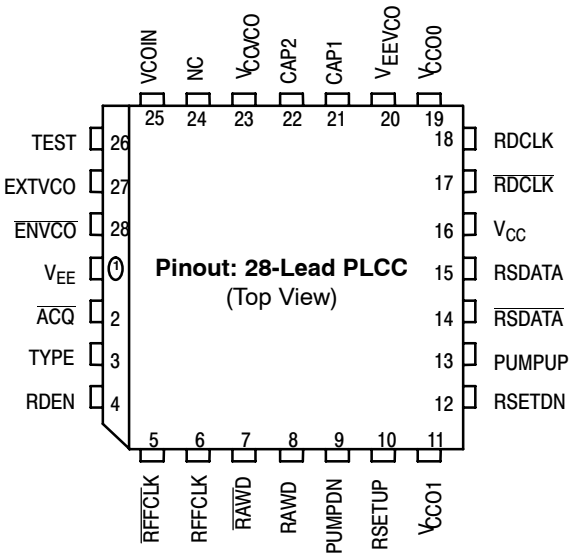
MARKING DIAGRAM



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10E197FN	PLCC−28	37 Units/Rail
MC10E197FNR2	PLCC−28	500 Units/Reel



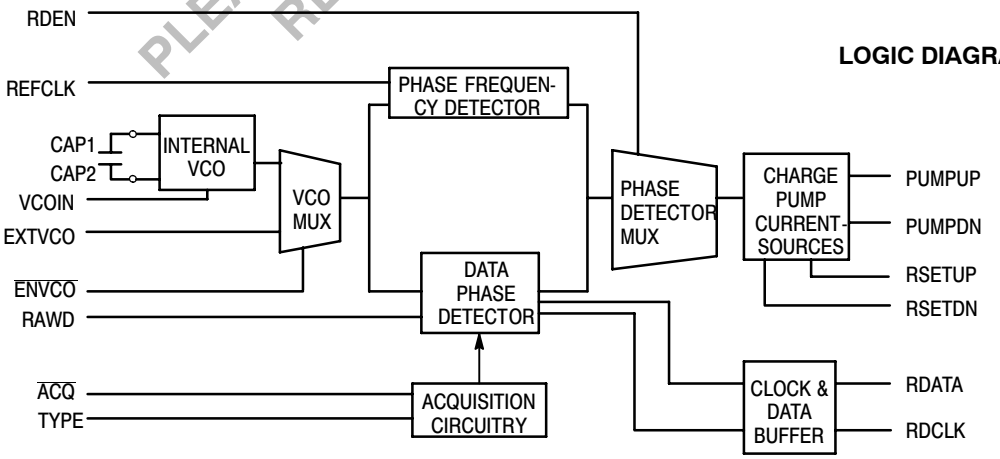
LOGIC DIAGRAM AND PINOUT ASSIGNMENT

* All V_{CC} and V_{CCOX} pins are tied together on the die.

Warning: All V_{CC}, V_{CCO}, and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

PIN DESCRIPTIONS

PIN	FUNCTION
REFCLK	ECL Reference clock equivalent to one clock cycle per decoding window.
REFCLK	ECL Reference clock equivalent to one clock cycle per decoding window.
RDEN	ECL Enable data synchronizer when HIGH. When LOW enable the phase/frequency detector steered by REFCLK.
RAWD	ECL Data Input to Synchronizer logic.
VCOIN	ECL VCO control voltage input
CAP1/CAP2	ECL VCO frequency controlling capacitor inputs
$\overline{\text{ENVCO}}$	ECL VCO select pin. LOW selects the internal VCO and HIGH selects the external VCO input. Pin floats LOW when left open.
EXTVCO	ECL External VCO pin selected when ENVCO is HIGH
$\overline{\text{ACQ}}$	ECL Acquisition circuitry select pin. This pin must be driven HIGH at the end of the data sync field for some sync field types.
TYPE	ECL Selects between the two types of commonly used sync fields. When LOW it selects a sync field interspersed with 3 zeroes (2:7 RLL code). When HIGH it selects a sync field interspersed with 2 zeroes (1:7 RLL code).
TEST	ECL Input included to initialize the clock flip-flop for test purposes only. Pin should be left open (LOW) in actual application.
PUMPUP	ECL Open collector charge pump output for the signal pump
PUMPDN	ECL Open collector charge pump output for the reference pump
RSETUP	ECL Current setting resistor for the signal pump
RSETDN	ECL Current setting resistor for the reference pump
RDATA	ECL Synchronized data output
RDCLK	ECL Synchronized clock output
V_{CC}, V^{CCOX}, V_{CCVCO}	Most positive supply rails. Digital and analog supplies are independent on chip
V_{EE}, V_{EEVCO}	Most negative supply rails. Digital and analog supplies are independent on chip



LOGIC DIAGRAM

MAXIMUM RATINGS (Note 1)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		8	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		−8	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 −6	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
TA	Operating Temperature Range			0 to +85	°C
T_{stg}	Storage Temperature Range			−65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	28 PLCC 28 PLCC	63.5 43.5	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	28 PLCC	22 to 26	°C/W
V_{EE}	PECL Operating Range NECL Operating Range			4.2 to 5.7 −5.7 to −4.2	V V
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

10E SERIES PECL DC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V (Note 1)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current	90	150	180	90	150	180	90	150	180	mA
V_{OH}	Output HIGH Voltage (Note 2)	3980	4070	4160	4020	4105	4190	4090	4185	4280	mV
V_{OL}	Output LOW Voltage (Note 2)	3050	3210	3370	3050	3210	3370	3050	3227	3405	mV
V_{IH}	Input HIGH Voltage	3830	3995	4160	3870	4030	4190	3940	4110	4280	mV
V_{IL}	Input LOW Voltage	3050	3285	3520	3050	3285	3520	3050	3302	3555	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.3	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.
1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / −0.06 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}−2 volts.

10E SERIES NECL DC CHARACTERISTICS V_{CCx}= 0.0 V; V_{EE}= −5.0 V (Note 1)

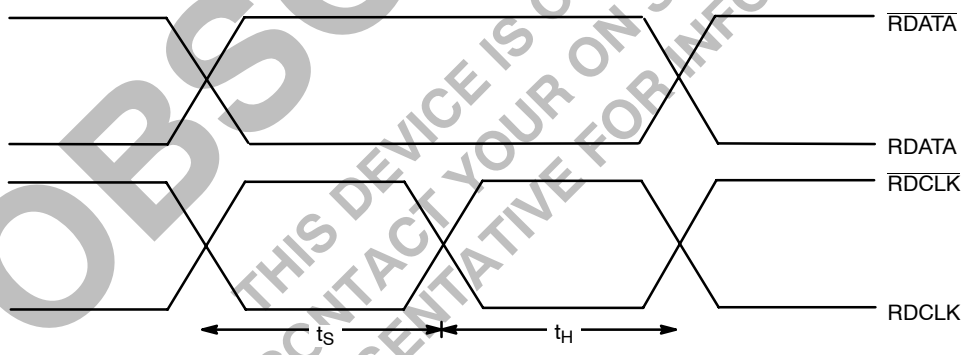
		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current	90	150	180	90	150	180	90	150	180	mA
V_{OH}	Output HIGH Voltage (Note 2)	−1020	−930	−840	−980	−895	−810	−910	−815	−720	mV
V_{OL}	Output LOW Voltage (Note 2)	−1950	−1790	−1630	−1950	−1790	−1630	−1950	−1773	−1595	mV
V_{IH}	Input HIGH Voltage	−1170	−1005	−840	−1130	−970	−810	−1060	−890	−720	mV
V_{IL}	Input LOW Voltage	−1950	−1715	−1480	−1950	−1715	−1480	−1950	−1698	−1445	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.065		0.3	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.
1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / −0.06 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}−2 volts.

AC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V or V_{CCx}= 0.0 V; V_{EE}= −5.0 V (Note 1)

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{VCO}	Frequency of the VCO (Note 5)	150			150			150			MH-z
	Tuning Ratio (Note 6)	1.53		1.87	1.53		1.87	1.53		1.87	
t_s	Time from RDATA Valid to Rising Edge of RDCLK (Notes 4)	T_{VCO} – 550			T_{VCO} – 500			T_{VCO} – 500			ps
t_H	Time from Rising Edge of RDCLK to RDATA invalid (Notes 4)	T_{VCO}			T_{VCO}			T_{VCO}			ps
t_{SKEW}	Skew Between RDATA and $\overline{RDATA}$			300			300			300	ps
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps

1. V_{EE} can vary +0.46 V / −0.06 V
1 Applies to the input current for each input except VCOIN
2 For a nominal set current of 3.72 mA, the resistor values for RSETUP and RSETDN should be 130Ω(0.1%). Assuming no variation between these two resistors, the current match between the PUMPUP and PUMPDN output signals should be within ±3%. I_{SET} is calculated as (V_{EE}+ 1.3v – V_{BE})/R; where R is RSETUP or RSETDN and a nominal value for V_{BE} is 0.85 volts.
3 Output leakage current of the PUMPUP or PUMPDN output signals when at a LOW level.
4 T_{VCO} is the period of the VCO.
5 The VCO frequency determined with VCOIN = V_{EE} + 0.5 volts and using a 10pF tuning capacitor.
6 The tuning ratio is defined as the ratio of f_{VCOMAX} to F_{VCOMIN} where f_{VCOMAX} is measured at VCOIN = 1.3 V + V_{EE} and f_{VCOMAX} is measured at VCOIN = 2.6 V + V_{EE}



SETUP AND HOLD TIMING DIAGRAMS

APPLICATIONS INFORMATION

General Operation

Operation

The E197 is a phase-locked loop circuit consisting of an internal VCO, a Data Phase detector with associated acquisition circuitry, and a Phase/Frequency detector (Figure 1). In addition, an enable pin(ENVCO) is provided to disable the internal VCO and enable the external VCO input. Hence, the user has the option of supplying the VCO signal.

The E197 contains two phase detectors: a data phase detector for synchronizing to the non-periodic pulses in the read data stream during the data read mode of operation, and a phase/ frequency detector for frequency (and phase) locking to an external reference clock during the "idle" mode of operation. The read enable (RDEN) pin muxes between these two detectors.

Data Read Mode

The data pins (RAWD) are enabled when the RDEN pin is placed at a logic high level, thus enabling the Data Phase detector (Figure1) and initiating the data read mode. In this mode, the loop is servoed by the timing information taken from the positive edges of the input data pulses. This phase detector samples positive edges from the RAWD signal and generates both a pump up and pump down pulse from any edge of the input data pulse. The leading edge of the pump up pulse is time modulated by the leading edge of the data signal, whereas the rising edge of the pump up pulse is generated synchronous to the VCO clock. The falling edge of the pump down pulse is synchronous to the falling edge of the VCO clock and the rising edge of the pump down signal is synchronous to the rising edge of the VCO clock. Since both edges of the VCO are used the internal clock a duty cycle of 50%. This pulse width modulation technique is used to generate the servoing signal which drives the VCO. The pump down signal is a reference pulse which is included to provide an evenly balanced differential system, thereby allowing the synthesis of a VCO input control signal after appropriate signal processing by the loop filter.

By using suitable external filter circuitry, a control signal for input into the VCO can be generated by inverting the pump down signal, summing the inverted signal with the pump up signal and averaging the result. The polarity of this control signal is defined as zero when the data edges lead the clock by a half clock cycle. If the data edges are advanced with respect to the zero polarity data/VCO edge relationship, the control signal is defined to have a negative polarity; whereas if the VCO is advanced with respect to the zero polarity data/VCO edge relationship, the control signal is defined to have a positive polarity. If there is no data edge present at the RAWD input, the corresponding pump up and pump down outputs are not generated and the resulting control output is zero.

Acquisition Circuitry

The acquisition circuitry is provided to assist the data phase detector in phase locking to the sync field that precedes the data. For the case in which lock-up is attempted when the data edges are coincident with the VCO edges, the pump down signal may enter an indeterminate state for an unacceptably long period due to the violation of internal set up and hold times. After an initial pump down pulse, the circuit blocks successive pump down pulses, and inserts extra pump up pulses, during portions of the sync field that are known to contain zeros. Thus, the data phase detector is forced to have a nonzero output during the lock-up period, and the restoring force ensures correction of the loop within an acceptable time. Hence, this circuitry provides a quasi-deterministic pump down output signal, under the condition of coincident data and VCO edges, allowing lock-up to occur with excessive delays.

The $\overline{ACQ}$ line is provided to disable (disable = HIGH) the acquisition circuit during the data portion of a sector block. Typically, this circuit is enabled at the beginning of the sync field by a one-shot timer to ensure a timely lock-up.

The TYPE line allows the choice between two sync field preamble types; transitions interspersed with two zeros between transitions. These types of sync fields are used with the 1:7 and 2:7 coding schemes, respectively.

Idle Mode

In the absence of data or when the drive is writing to the disk, PLL servoing is accomplished by pulling the read enable line (RDEN) low and providing a reference clock via the REFCLK pins. The condition whereby RDEN is low selects the Phase/Frequency detector (Figure 1) and the 10E197 is said to be operating in the "idle mode". In order to function as a frequency detector the input waveform must be periodic. The pump up and pump down pulses from the Phase/Frequency detector will have the same frequency, phase and pulse width only when the two clocks that are being compared have their positive edges aligned and are of the same frequency.

As with the data phase detector, by using suitable external filter circuitry, a VCO input control signal can be generated by inverting the pump down signal, summing the inverted signal with the pump up signal and averaging the result. The polarity of this control signal is defined as zero when all positive edges of both clocks are coincident. For the case in which the frequencies of the two clocks are the same but the clock edges of the reference clock are slightly advanced with respect to the VCO clock, the control clock is defined to have a positive polarity. A control signal with negative polarity occurs when the edges of the reference clock are delayed with respect to those of the VCO. If the frequencies of the two clocks are different, the clock with the most edges per unit time will initiate the most pulses and the polarity of the detector will reflect the frequency error. Thus, when the reference clock is high in frequency than the VCO clock the polarity of the control signal is positive; whereas a control signal with negative polarity occurs when the frequency of the reference clock is lower than the VCO clock.

Phase-Lock Loop Theory

Introduction

Phase lock loop (PLL) circuits are fundamentally feedback systems used to synchronize the frequency of an oscillator to an incoming signal. In addition to frequency synchronization, the PLL circuitry is designed to minimize the phase difference between the system input and output signals. A block diagram of a feedback control system is shown in Figure 1.

where:

A(s) is the product of the feed-forward transfer functions.

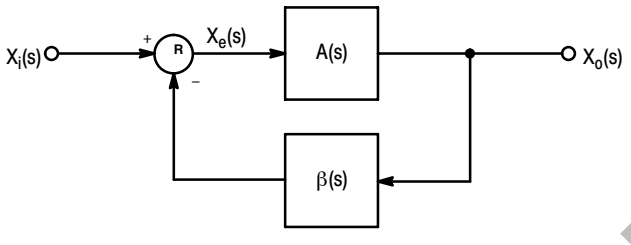


Figure 1. Feedback System

β(s) is the product of the feedback transfer functions.

The transfer function for this closed loop system is

$$\frac{X_o(s)}{X_i(s)} = \frac{A(s)}{1 + A(s)\beta(s)}$$

Typically, phase lock loops are modeled as feedback systems connected in a unity feedback configuration (β(s)=1) with a phase detector, a VCO (voltage controlled oscillator), and a loop filter in the feed-forward path, A(s). Figure 2 illustrates a phase lock loop as a feedback control system in block diagram form.

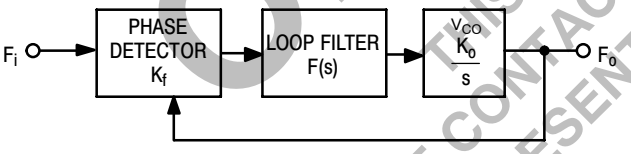


Figure 2. Phase Lock Loop Block Diagram

The closed loop transfer function is:

$$\frac{X_o(s)}{X_i(s)} = \frac{K_\phi \frac{K_o}{s} F(s)}{1 + K_\phi \frac{K_o}{s} F(s)}$$

where:

K_ϕ= the phase detector gain.
K_o= the VCO gain. Since the VCO introduces a pole at the origin of the s-plane, K_o is divided by s.
F(s) = the transfer function of the loop filter.

The 10E197 is designed to implement the phase detector and VCO functions in a unity feedback loop, while allowing the user to select the desired filter function.

Gain Constants

As mentioned, each of the three sections in the phase lock loop block diagram has an associated open loop gain constant. Further, the gain constant of the filter circuitry is composed of the product of three gain constants, one for each filter subsection. The open loop gain constant of the feed-forward path is given by

$$K_{ol} = K_\phi * K_o * K_1 * K_l * K_d \qquad \text{eqt. 1}$$

and obtained by performing a root locus analysis.

Phase Detector Gain Constant

The gain of the phase detector is a function of the operating mode and the data pattern. The 10E197 provides data separation for signals encoded in 2:7 or 1:7 RLL encoding schemes; hence, Tables 1 and 2 are coding tables for these schemes. Table 3 lists nominal phase detector gains for both 2:7 and 1:7 sync fields.

NRZ Data Sequence	Code Sequence
00	1000
01	0100
100	001000
101	100100
111	000100
1100	00001000
1101	00100100

Table 1. 2:7 RLL Encoding Table

NRZ Data Sequence	Code Sequence
00	X01
01	010
10	X00
1100	010001
1101	X00000
1110	X00001
1111	010000

An X in the leading bit of a code sequence is assigned the complement of the bit

Table 2. 1:7 RLL Encoding Table

Sync Pattern	Read Mode	Idle Mode
2:7	121 mV/radian	484 mV/radian
1:7	161 mV/radian	483 mV/radian

Table 3. Phase Detector Gain Constants

VCO Gain Constant

The gain of the VCO is a function of the tuning capacitor. For a value of 10 pF a nominal value of the gain, K_o, is 20 MHz per volt.

Filter Circuitry Gain Constant(s)

The open loop gain constant of the filter circuitry is given by:

$$K_{fc} = K_1 * K_l * K_d \qquad \text{eqt. 2}$$

The individual gain constants are defined in the appropriate subsections of this document.

Loop Filter

The two major functions of the loop filter are to remove any noise or high frequency components present in the phase detector output signal and, more importantly, to control the characteristics which determine the dynamic response of the phase lock loop; i.e. capture range, loop bandwidth, capture time, and transient response.

Although a variety of loop filter configurations exist, this section will only describe a filter capable of performing the signal processing as described in the Data Read Mode and the Idle Mode sections. The loop filter consists of a differential summing amplifier cascaded with an augmenting integrator which drives the VCOIN input to the 10E197 through a resistor divider network (Figure 3).

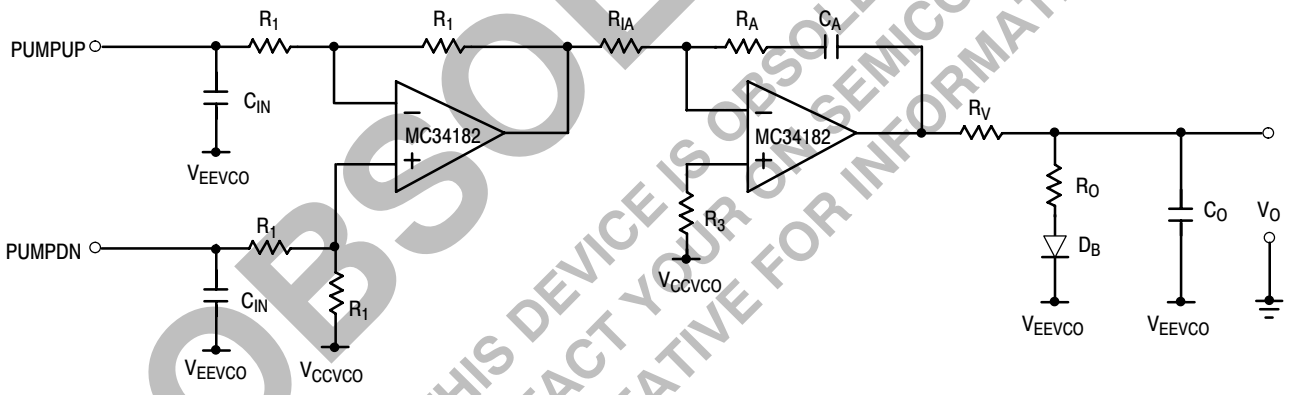


Figure 3. Loop Filter Circuitry

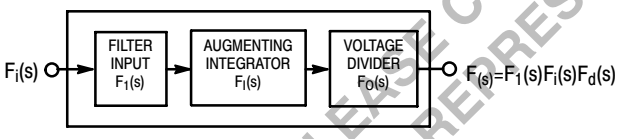


Figure 4. Loop Filter Block Diagram

A root locus analysis is performed on the open loop transfer function to determine the final pole-zero locations and the open loop gain constant for the phase lock loop. Note that the open loop gain constant impacts the crossover frequency and that a lower frequency crossover point means a much more efficient filter. Once these positions and constants are determined the component values may be calculated.

The transfer function and the element values for the loop filter are derived by dividing the filter into three cascaded subsections: filter input, augmenting integrator, and the voltage divider network (Figure 4).

Loop Filter Transfer Function

The open loop transfer function of the phase lock loop is the product of each individual filter subsection, as well as the phase detector and VCO. Thus, the open loop filter transfer function is:

$$F_o(s) = K_\phi * \frac{K_o}{s} * F_1(s) * F_l(s) * F_d(s)$$

where:

$$F_1(s) = K_1 * \frac{1}{(s + p_1)} * \frac{1}{[s^2 + (2\zeta\omega_{o1})\, s + \omega^2_{o1}]}$$

$$F_l(s) = K_l * \frac{1}{s} * \frac{(s + z)}{[s^2 + (2\zeta\omega_{o2})\, s + \omega^2_{o2}]}$$

$$F_d(s) = K_d * \frac{1}{(s + p_2)}$$

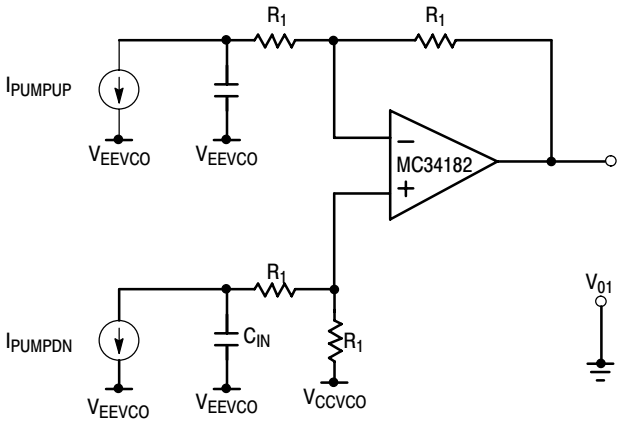


Figure 5. Filter Input Subsection

Filter Input

The primary function of the filter input subsection is to convert the output of the phase detector into a single ended signal for subsequent processing by the integrator circuitry. This subsection consists of the 10E197 charge pump current sinks, two shunt capacitors, and a differential summing amplifier (Figure 5).

Hence, this portion of the filter circuit contributes a real pole and two complex poles to the overall loop transfer function F(s). Before these pole locations are selected, appropriate values for the current setting resistors (RSETUP and RSETDN) must be ascertained. The goal in choosing these resistor values is to maximize the gain of the filter input subsection while ensuring the charge pump output transistors operate in the active mode. The filter input gain is maximized for a charge pump current of 1.1 mA; a value of 464 Ω for both RSETUP and RSETDN yields a nominal charge pump current of 1.1 mA.

It should be noted that a dual bandwidth implementation of the phase lock loop may be achieved by modifying the current setting resistors such that an electronic switch enables one of two resistor configurations. Figure 6 shows a circuit configuration capable of providing this dual bandwidth function. Analysis of the filter input circuitry yields the transfer function:

$$F_1(s) = K_1 * \frac{1}{(s + p_1)} * \frac{1}{[s^2 + (2\zeta\omega_{o1})\, s + \omega_{o1}^2]}$$

The gain constant is defined as:

$$K_1 = A_1 * \frac{1}{C_{IN}} \qquad \text{eqt. 3}$$

where:

A_1 = op-amp gain constant for the selected pole positions.

C_{IN} = phase detector shunt capacitor.

The real pole is a function of the input resistance to the op-amp and the shunt capacitors connected to the phase detector output. For stability the real pole must be placed beyond the unity gain frequency; hence, this pole is typically placed midway between the unity crossover and phase detector sampling frequency, which should be about ten times greater.

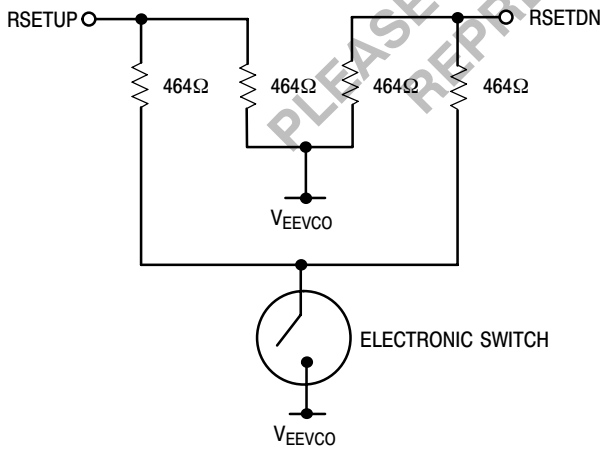


Figure 6. Dual Bandwidth Current Source Implementation

The second order pole set arises from the two pole model for an op-amp. The open loop gain and the first open loop pole for the op-amp are obtained from the data sheets. Typically, op-amp manufacturers do not provide information on the location of the second open loop pole; however, it can be approximated by measuring the roll off of the op-amp in the open loop configuration. The second pole is located where the gain begins to decrease at a rate of 40 dB per decade. The inclusion of both poles in the differential summing amplifier transfer function becomes important when closing the feedback path around the op-amp because the poles migrate; and this migration must be accounted for to accurately determine the phase lock loop transient performance.

Typically the op-amp poles can be approximated by a pole pair occurring as a complex conjugate pair making an angle of 45° to the real axis of the complex frequency plane. Two constraints on the selection of the op-amp pole pair are that the poles lie beyond the crossover frequency and they are positioned for near unity gain operation. Performing a root locus analysis on the op-amp open loop configuration and adhering to the two constraints yields the pole positions contributed by the op-amp.

Determination of Element Values

Since the difference amplifier is configured to operate as a differential summer the resistor values associated with the amplifier are of equal value. Further, the typical input resistance to the summing amplifier is 1 kΩ; thus, the op-amp resistors are set at 1 kΩ. Having set the input resistance to the op-amp and selected the position of the real pole, the value of the shunt capacitors is determined using the following relationship:

$$|p_1| = \frac{1}{2\pi R_1 C_{IN}} \qquad \text{eqt. 4}$$

Augmenting Integrator

The augmenting integrator consists of an active filter with a lag-lead network in the feedback path (Figure 7).

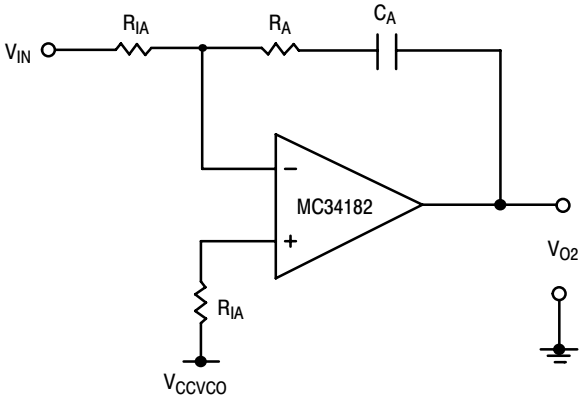


Figure 7. Integrator Subsection

Analysis of this portion of the filter circuit yields the transfer function:

$$F_1(s) = K_I * \frac{1}{s} * \frac{(s + z)}{[s^2 + (2\zeta\omega_{o2})\, s + \omega^2_{o2}]}$$

The gain constant is defined as:

$$K_I = A_I * \frac{R_A}{R_{IA}} \qquad \text{eqt. 5}$$

where:

A_I = op-amp gain constant for selected pole positions.

R_A = integrator feedback resistor.

R_{IA} = integrator input resistor.

The integrator circuit introduces a zero, a pole at the origin, and a second order pole set as described by the two pole model for an op-amp. As in the case of the differential summing amplifier, we assume the op-amp pole pair occur as a complex conjugate pair making an angle of 45° to the real axis of the complex frequency plane; are positioned for near unity gain operation; and are located beyond the crossover frequency. Since both the summing and integrating op-amps are realized by the same type of op-amp (MC34182D), the open loop pole positions for both amplifiers will be the same.

Further, the loop transfer function contains two poles located at the origin, one introduced by the integrator and the other by the VCO; hence a zero is necessary to compensate for the phase shift produced by these poles and ensure loop stability. The op-amp will be stable if the crossover point occurs before the transfer function phase angle becomes 180°. The zero should be positioned much less than one decade before the unity gain frequency.

As in the case of the filter input circuitry, the poles and zero from this analysis will be used as open loop poles and a zero when performing the root locus analysis for the complete system.

Determination of Element Values

The location of the zero is used to determine the element values for the augmenting integrator. The value of the capacitor, C_A, is selected to provide adequate charge storage when the loop is not sampling data. A value of 0.1 μF is sufficient for most applications; this value may be increased when the RDCLK frequency is much lower than 4 MHz. The value of R_A is governed by:

$$|z| = \frac{1}{2\pi R_A C_A} \qquad \text{eqt. 6}$$

For unity gain operation of the integrating op-amp the value of RIA is selected such that:

$$R_{IA} = R_A \qquad \text{eqt. 7}$$

It should be noted that although the zero can be tuned by varying either R_A or C_A, caution must be exercised when adjusting the zero by varying C_A because the integrator gain is also a function of C_A. Further, the gain of the loop filter can be adjusted by changing the integrator input resistor R_{IA}.

Voltage Divider

The input range to the VCOIN input is from 1.3 V + V_{EE} to 2.6 V + V_{EE}; hence, the output from the augmenting amplifier section must be attenuated to meet the VCOIN constraints. A simple voltage divider network provides the necessary attenuation (Figure 8).

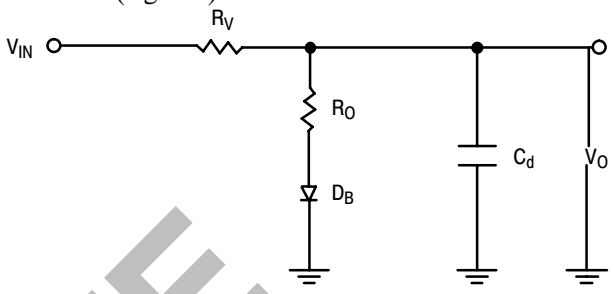


Figure 8. Voltage Divider Subsection

In addition, a shunt filter capacitor connected between the VCOIN input pin and V_{EE} provides the voltage divider subsection with a single time constant transfer function that adds a pole to the overall loop filter. The transfer function for the voltage divider network is:

$$F_d(s) = K_d * \frac{1}{(s + p_2)}$$

The gain constant, K_d, is defined as:

$$K_d = \frac{1}{R_v C_d} \qquad \text{eqt. 9}$$

he value of K_d is easily extracted by rearranging Equation 1:

$$K_d = \frac{K_{ol}}{K_\phi * K_o * K_1 * K_I} \qquad \text{eqt. 10}$$

The gain constant K_d is set such that the output from the integrator circuit is within the range 1.3 V +V_{EE} to 2.6 V +V_{EE}. The pole for the voltage divider network should be positioned an octave beyond that for the filter input.

Determination of Element Values

Once the pole location and the gain constant K_d are established the resistor values for the voltage divider network are determined using the design guidelines mentioned above and from the following relationship:

$$\frac{K_d}{2\pi |p_2|} = \frac{R_o}{R_o + R_v}$$

Having determined the resistor values, the filter capacitor is calculated by rearranging Equation 9:

$$C_d = \frac{1}{R_v K_d} \qquad \text{eqt. 9a}$$

Finally, a bias diode is included in the voltage divider network to provide temperature compensation. The finite resistance of this diode is neglected for these calculations.

Calculations For a 2:7 Coding Scheme

Introduction

The circuit component values are calculated for a 2:7 coding scheme employing a data rate of 23 Mbit/sec. Since the number of bits is doubled when the data is encoded, the data clock is at half the frequency of the RDCLK signal. Thus, the operating frequency for these calculations is 46 MHz. Further, the pole and zero positions are a function of the data rate; hence, the component values derived by these calculations must be scaled if a different operating frequency is used. Finally, it should be noted that the values are optimized for settling time.

The analysis is divided into three parts: static pole positioning, dynamic pole positioning, and dynamic zero positioning. Dynamic poles and zeros are those which the designer may position, to yield the desired dynamic response, through the judicious choice of element values. Static poles are not directly controlled by the choice of component values.

Static Poles

Each op-amp introduces a pair of "static" complex conjugate poles which must lie beyond the crossover frequency. As obtained from the data sheets and laboratory measurements, the two open loop poles for the MC34182D are:

$$P^*_{1a} = -0.1\text{Hz}$$

$$P^*_{1b} = -11.2\text{Hz}$$

Performing a root locus analysis and following the two guidelines previously stated, an acceptable pole set is:

$$P_{1a} = -5.65 + j5.65\text{MHz}$$

$$P_{1b} = -5.65 - j5.65\text{MHz}$$

Both op-amps introduce a set of static complex conjugate poles at these positions for a total of four poles. Further, the loop gain for each op-amp associated with these pole positions is determined from the root locus analysis to be:

$$A_1 = A_2 = 2.48\ e15\ \frac{V}{V}$$

In addition to the op-amps, the integrator and the VCO each contribute a static pole at the origin. Thus, there are a total of six static poles.

Dynamic Poles

The filter input and the voltage divider sections each contribute a dynamic pole. As stated previously, the filter input pole should be positioned midway between the unity crossover point and the phase detector sampling frequency. Hence, the open loop filter input pole position is selected as:

$$P^*_1 = -1.24\text{MHz}$$

The voltage divider pole is set approximately one octave higher than the filter input pole. Thus the open loop voltage divider pole position is picked to be:

$$P^*_2 = -2.57\text{MHz}$$

Dynamic Zero

Finally, the zero is positioned much less than one decade before the crossover frequency; for this design the zero is placed at:

$$z = -311\text{Hz}$$

Once the dynamic pole and zero positions have been determined, the phase margin is determined using a Bode plot; if the phase margin is not sufficient, the dynamic poles may be moved to improve the phase margin. Finally, a root locus analysis is performed to obtain the optimum closed loop pole positions for the dynamic characteristics of interest.

Component Values

Having determined the closed loop pole and zero positions the component values are calculated. From the root locus analysis the dynamic pole and zero positions are:

$$P_1 = -573\text{kHz}$$

$$P_2 = -3.06\text{MHz}$$

$$z = -311\text{Hz}$$

Filter Input Subsection

Rearranging Equation 4:

$$C_{IN} = \frac{1}{2\pi R_1 |P_1|}$$

and substituting 573 kHz for the pole position and 1 kΩ for the resistor value yields:

$$C_{IN} = 278\ \text{pF}$$

Augmenting Integrator Subsection

Rearranging Equation 6:

$$R_A = \frac{1}{2\pi |z| C_A}$$

and substituting 311 Hz for the zero position and 0.1 μF for the capacitor value yields:

$$R_A = 5.11\text{k}\Omega$$

From Equation 7 the value for the other resistors associated with the integrator op-amp are set equal to R_A:

$$R_{IA} = R_A = 5.11\text{k}\Omega$$

Voltage Divider Subsection

The element values for the voltage divider network are calculated using the relationships presented in Equations 8, 9, and 10 with the constraint that this divider network must produce a voltage that lies within the range 1.3 V + V_{EE} to 2.6 V + V_{EE}.

Restating Equation 9,

$$K_d = \frac{K_{ol}}{K_\phi * K_o * K_1 * K_l}$$

From the root locus analysis K_{ol} is determined to be:

$$K_{ol} = 1.585\ e51\ \frac{V}{mA\ sec^3}$$

From Equation 3

$$K_1 = A_1 * \frac{1}{C_{IN}}$$

and the gain constant K_1 is:

$$K_1 = 8.90\ e21\ \frac{V}{mA\ sec}$$

From Equation 5

$$K_l = A_l * \frac{R_A}{R_{IA}}$$

and the gain constant K_l is:

$$K_l = 2.48\ e15\ \frac{V}{V}$$

Having determined the gain constant K_d , the value of R_v, is selected such that the constraints $R_v > R_o$ and:

$$\frac{K_d}{2\pi |P_2|} = \frac{R_o}{R_o + R_v}$$

are fulfilled. The pole position P_2 is determined from the root locus analysis to be:

$$P_2 = -3.06MHz$$

Hence, R_v is selected to be:

$$R_v = 2.15k\Omega$$

and R_o is calculated to be:

$$R_o = 700\Omega$$

Finally, using Equation 8a:

$$C_d = \frac{1}{R_v K_d} \qquad \text{eqt. 8a}$$

the capacitor value, C_d is:

$$C_d = 98pF$$

Note that the voltage divider section can be used to set the gain, but the designer is cautioned to be sure the input value to VCOIN is within the correct range.

Component Scaling

As mentioned, these design equations were developed for a data rate of 23 Mbit/sec. If the data rate is different from the nominal design value the reactive elements must be scaled accordingly. The following equations are provided to facilitate scaling and were derived with the assumptions that a 2:7 coding scheme is used and that the RDCLK signal is twice the frequency of the data clock.

$$C_{IN} = 278 * \frac{46}{f} \quad (pF) \qquad \text{eqt. 11}$$

$$C_d = 98 * \frac{46}{f} \quad (pF) \qquad \text{eqt. 12}$$

where f is the RDCLK frequency in MHz.

Example for an 11 Mbit/sec Data Rate

As an example of scaling, assume the given filter and a 2:7 code are used but the data rate is 11 Mbit/sec. The dynamic pole positions, and therefore the bandwidth of the loop filter, are a function of the data rate. Thus a slower data rate will force the dynamic poles and the bandwidth to move to a lower frequency. From Equation 11 the value of C_{IN} is:

$$C_{IN} = 581pF$$

and from Equation 12 the value of C_d is:

$$C_d = 205pF$$

Thus the element values for the filter are:

Filter Input Subsection:

$$C_{IN} = 581pF$$

$$R_1 = 1k\Omega$$

Integrator Subsection:

$$C_A = 0.1\mu F$$

$$R_A = 5.11k\Omega$$

$$R_{IA} = 5.11k\Omega$$

Voltage Divider Subsection:

$$C_d = 205pF$$

$$R_v = 2.15k\Omega$$

$$R_o = 700k\Omega$$

Note, the poles P_1 and P_2 are now located at:

$$P_1 = -274kHz$$

$$P_2 = -1.47MHz$$

And, the open loop filter unity crossover point is at 300 kHz. The gain can be adjusted by changing the value of R_{IA} and the value of C_d. Varying the gain by changing C_d is not recommended because this will also move the poles, hence affect the dynamic 2 performance of the filter.

Calculations For a 1:7 Coding Scheme

Introduction

The circuit component values are calculated for a 1:7 coding scheme employing a data rate of 20 Mbit/sec. Since the number of bits increases from two to three when the data is encoded, the data clock is at two-thirds the frequency of the RDCLK signal. Thus, the operating frequency for these calculations is 30 MHz. As in the case of the 2:7 coding scheme the pole and zero positions are a function of the data rate, hence the component values derived by these calculations must be scaled if a different operating frequency is used.

Again, the analysis is divided into three parts: static pole positioning, dynamic pole positioning, and dynamic zero positioning.

Static Poles

As in the 2:7 coding example, an MC34182D op-amp is employed, hence the pole set is:

$$P_{1a} = -5.65 + j5.65\text{MHz}$$

$$P_{1b} = -5.65 - j5.65\text{MHz}$$

and the open loop gain is:

$$A_I = A_2 = 2.48\ e15\ \frac{V}{V}$$

Since the op-amps introduce a set of complex conjugate poles, a total of four poles are introduced by the op-amp. In addition, the integrator and the VCO each contribute a pole at the origin for a total of six static poles.

Dynamic Poles

The filter input and the voltage divider sections each contribute a dynamic pole. As stated previously, the filter input pole should be positioned midway between the unity crossover point and the phase detector sampling frequency. Hence, the open loop filter input pole position is selected as:

$$P^*_1 = -1.1\text{MHz}$$

The voltage divider pole is set approximately one octave higher than the filter input pole. Thus, the open loop voltage divider pole position is selected as:

$$P^*_2 = -2.28\text{MHz}$$

Dynamic Zero

Finally, the zero is positioned much less than one decade before the crossover frequency; for this design the zero is placed at:

$$z = -311\text{Hz}$$

Once the dynamic pole and zero positions have been determined, the phase margin is determined using a Bode plot; if the phase margin is not sufficient, the dynamic poles may be moved to improve the phase margin. Finally, a root locus analysis is performed to obtain the optimum closed loop pole positions for the dynamic characteristics of interest.

Component Values

Having determined the closed loop pole and zero positions the component values are calculated. From the root locus analysis the dynamic pole and zero positions are:

$$P_1 = -541\text{kHz}$$

$$P_2 = -2.73\text{MHz}$$

$$z = -311\text{Hz}$$

Filter Input Subsection

Rearranging Equation 4

$$C_{IN} = \frac{1}{2\pi R_1 |P_1|}$$

and substituting 541 kHz for the pole position and 1.0 kΩ for the resistor value yields:

$$C_{IN} = 294\ \text{pF}$$

Augmenting Integrator Subsection

Rearranging Equation 6

$$R_A = \frac{1}{2\pi |z| C_A}$$

and substituting 311 Hz for the zero position and 0.1 μF for the capacitor value yields:

$$R_A = 5.11\text{k}\Omega$$

From Equation 7 the value for the other resistors associated with the integrator op-amp are set equal to R_A:

$$R_{IA} = R_A = 5.11\text{k}\Omega$$

Voltage Divider Subsection

The element values for the voltage divider network are calculated using the relationships presented in Equations 8, 9, and 10 with the constraint that this divider network must produce a voltage that lies within the range 1.3 V + V_{EE} to 2.6 V + V_{EE}.

Restating Equation 9,

$$K_d = \frac{K_{ol}}{K_\phi * K_o * K_1 * K_I}$$

From the root locus analysis K_{ol} is determined to be:

$$K_{ol} = 1.258\ e51\ \frac{V}{MA\ SEC^3}$$

From Equation 3:

$$K_1 = A_1 * \frac{1}{C_{IN}}$$

and the gain constant K_1:

$$K_1 = 8.42\ e21\ \frac{V}{mA\ sec}$$

From Equation 5:

$$K_I = A_I * \frac{R_A}{R_{IA}}$$

and the gain constant K_I is:

$$K_I = 2.48\ e15\ \frac{V}{V}$$

$$K_d = 2.98\ e6\ sec^{-1}$$

Having determined the gain constant K_d , the value of R_v, is selected such that the constraints $R_v > R_o$ and:

$$\frac{K_d}{2\pi|p_2|} = \frac{R_o}{R_o + R_v}$$

are fulfilled. The pole position P_2 is determined from the root locus analysis to be:

$$P_2 = -2.73MHz$$

Hence, R_v is selected to be:

$$R_v = 2.15k\Omega$$

and R_o is calculated to be:

$$R_o = 453\Omega$$

Finally, using Equation 8a:

$$C_d = \frac{1}{R_v K_d} \qquad \text{eqt. 8a}$$

the capacitor value, C_d is calculated to be:

$$C_d = 156pF$$

Again, note the voltage divider section can be used to set the gain, but the designer is cautioned to be sure the input value to VCOIN is within the correct range.

Component Scaling

As mentioned, these design equations were developed for a data rate of 20 Mbit/sec. If the data rate is different from the nominal design value the reactive elements must be scaled accordingly. The following equations provided are to facilitate scaling and were derived with the assumptions that a 1:7 coding scheme is used and that the RDCLK signal is twice the frequency of the data clock:

$$C_{IN} = 294 * \frac{30}{f} \quad (pF) \qquad \text{eqt. 13}$$

$$C_d = 156 * \frac{30}{f} \quad (pF) \qquad \text{eqt. 14}$$

where f is the RDCLK frequency in MHz.

Example for an 10 Mbit/sec Data Rate

As an example of scaling, assume the given filter and a 1:7 code are used but the data rate is 10 Mbit/sec. The dynamic pole positions and, therefore, the bandwidth of the loop filter, are a function of the data rate. Thus, a slower data rate will force the dynamic poles and the bandwidth to move to a lower frequency. From Equation 13 the value of C_{IN} is:

$$C_{IN} = 588pF$$

and from Equation 14 the value of C_d is:

$$C_d = 312pF$$

Thus, the element values for the filter are:

Filter Input Subsection:

$$C_{IN} = 588pF$$

$$R_1 = 1.0k\Omega$$

Integrator Subsection:

$$C_A = 0.1\mu F$$

$$R_A = 5.11k\Omega$$

$$R_{IA} = 5.11k\Omega$$

Voltage Divider Subsection:

$$C_d = 312pF$$

$$R_v = 2.15k\Omega$$

$$R_o = 453k\Omega$$

Note, the poles P_1 and P_2 are now located at:

$$P_1 = -271kHz$$

$$P_2 = -1.36MHz$$

And, the open loop filter unity crossover point is at 300 kHz. As in the case of the 2:7 coding scheme, the gain can be adjusted by changing the value of R_{IA} and the value of C_d. Varying the gain by changing C_d is not recommended because this will also move the poles, hence affect the dynamic performance of the filter.

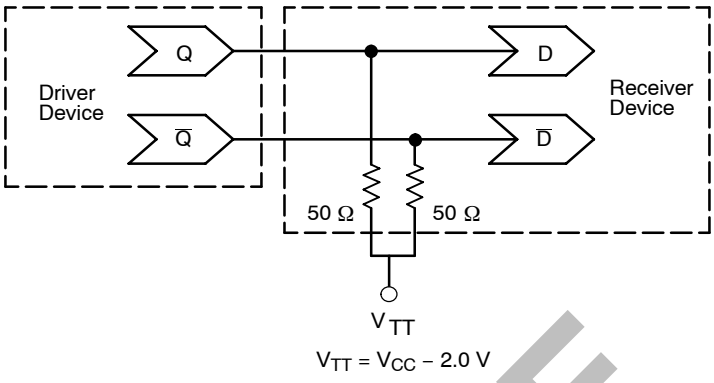


Figure 9. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404	–	ECLinPS Circuit Performance at Non–Standard V_{IH} Levels
AN1405	–	ECL Clock Distribution Techniques
AN1406	–	Designing with PECL (ECL at +5.0 V)
AN1503	–	ECLinPS I/O SPICE Modeling Kit
AN1504	–	Metastability and the ECLinPS Family
AN1568	–	Interfacing Between LVDS and ECL
AN1596	–	ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
AN1650	–	Using Wire–OR Ties in ECLinPS Designs
AN1672	–	The ECL Translator Guide
AND8001	–	Odd Number Counters Design
AND8002	–	Marking and Date Codes
AND8020	–	Termination of ECL Logic Devices

PACKAGE DIMENSIONS

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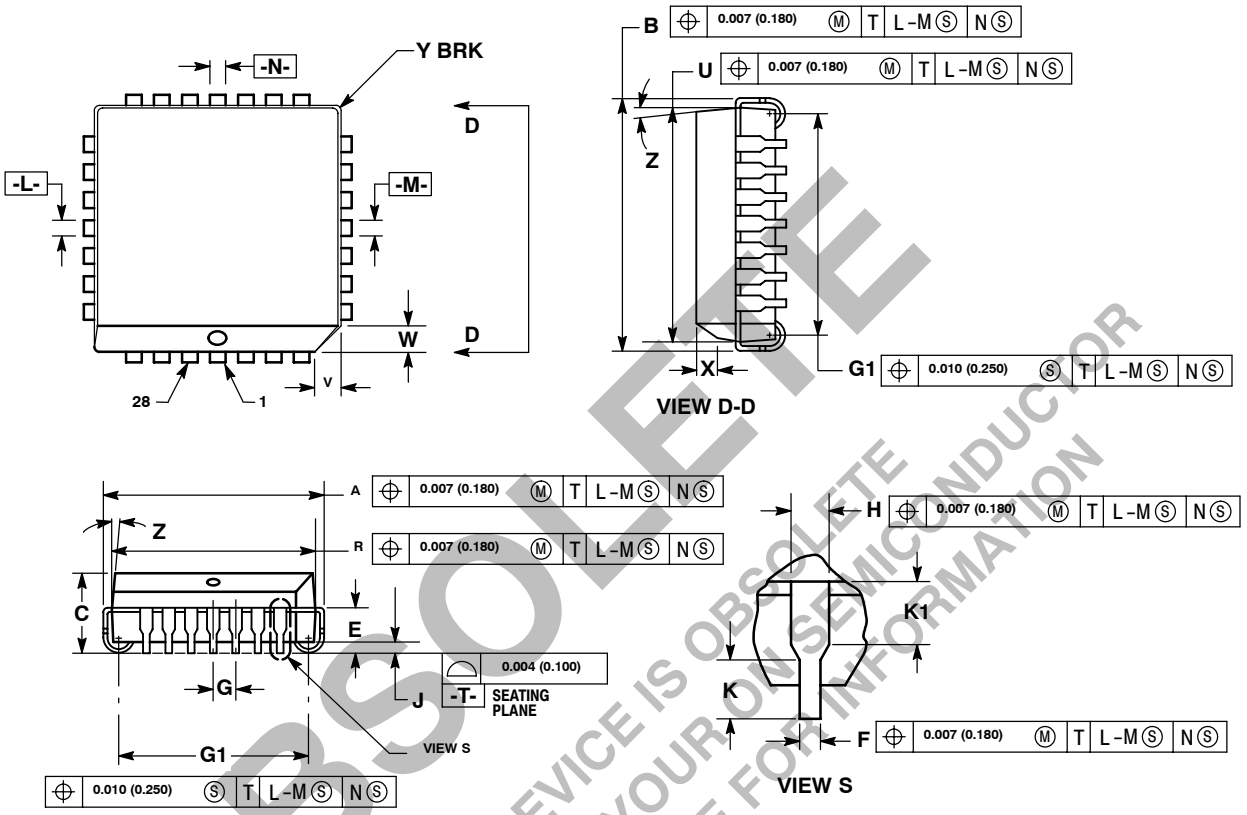
PLASTIC PLCC PACKAGE
CASE 776−02
ISSUE E



NOTES:
1. DATUMS -L-, -M-, AND -N- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
2. DIM G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
3. DIM R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.485	0.495	12.32	12.57
B	0.485	0.495	12.32	12.57
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	—	0.51	—
K	0.025	—	0.64	—
R	0.450	0.456	11.43	11.58
U	0.450	0.456	11.43	11.58
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	—	0.020	—	0.50
Z	2°	10°	2°	10°
G1	0.410	0.430	10.42	10.92
K1	0.040	—	1.02	—

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